Lab 15 finding

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ECEN 5730
PCB DESIGN

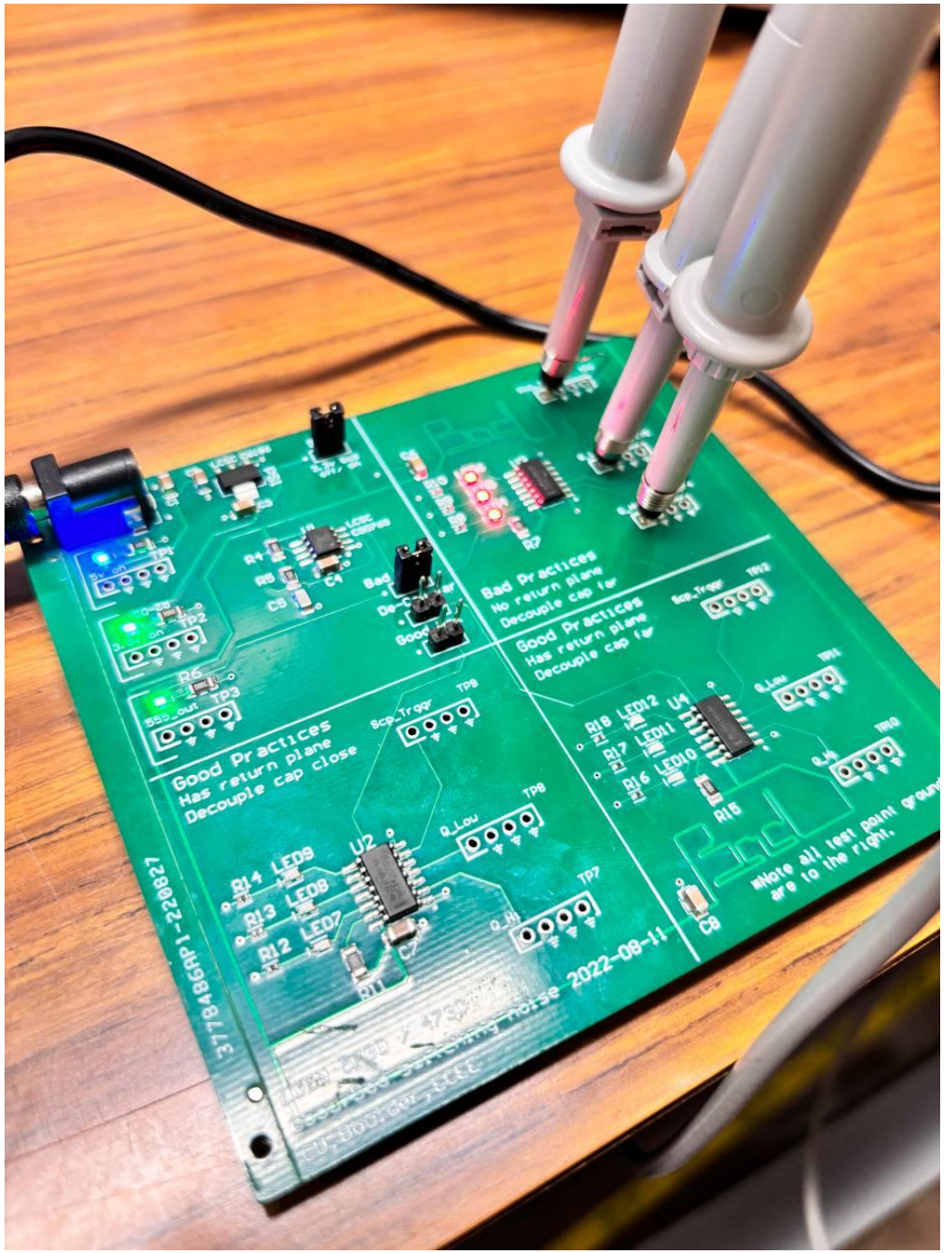
Data collected from a Hex inverter high speed digital circuit

Overview:
Good and bad switching noise

- Objective:
  To investigate how PCB layout (good vs. bad return path and decoupling) affects switching noise, rise time and fall time, and rail stability in high-speed digital circuits.
- This experiment demonstrates the importance of good layout practices, such as solid return planes and close decoupling, in minimizing noise and improving switching speed.

Overview of circuit:

- Quality_Metric: Compare the rise/fall times as well as the rail collapse of each of the three blocks
  - Good layout= Close decoupling, solid return plane
  - GOOD but Cap far = Far decoupling, solid return plane
  - Bad Bad = Far decoupling, no return plane



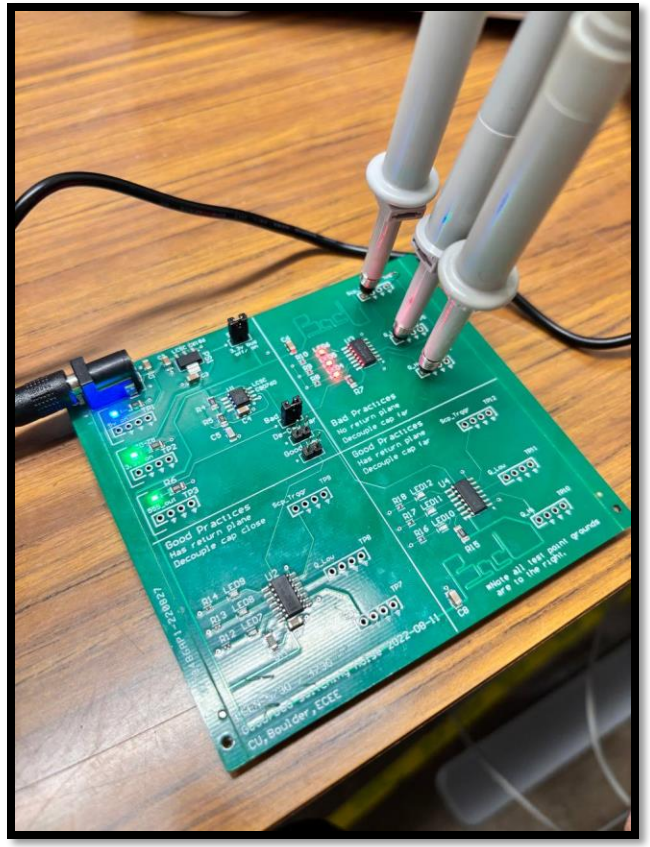
Key finding:

555 clock	Bad layout
Good layout	Good but cap far

Rise/fall times were measured for both good and bad PCB layouts using the 555-timer trigger.

Key message: Good layout → fast, clean transitions.
Bad layout → slower edges and larger rail noise from poor return paths and decoupling.

Layout	Rise Time (ns)	Vp-p Rail Collapse (mV)	Relative to Good Layout
Good Layout	2.25 ns	274	**Reference (1×)**
Good but Cap Far	3.77 ns	1031	**1.7× slower, 5× more noise**
Bad Layout	4.86 ns	709	**2.2× slower, 2.6× more noise**



Summary

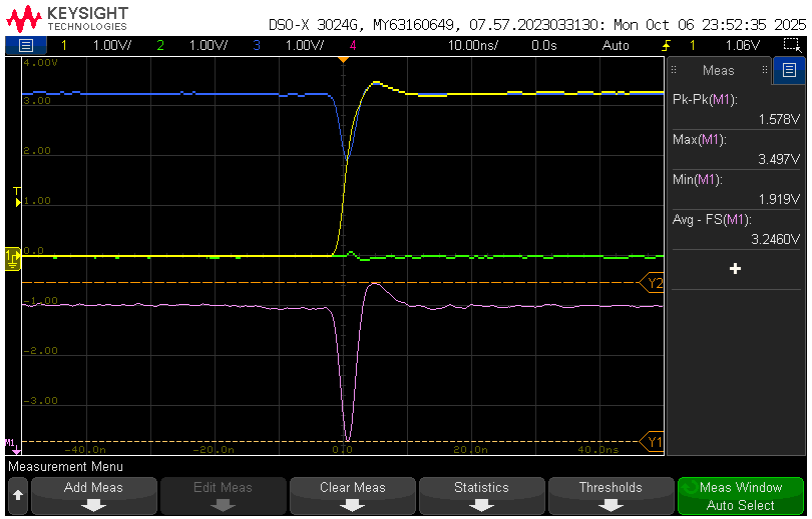
In this experiment, we measured how PCB layout quality affects switching speed and rail stability.

Despite identical circuits, layout differences caused significant variation in performance.

- The bad layout showed 2.2× slower rise time and nearly 2× higher rail noise compared to the good layout.
- The good but cap far layout also degraded performance, showing ~1.7× slower edges and larger rail collapse, confirming the importance of short decoupling paths.
- The good layout maintained the fastest transitions and most stable voltage rails due to proper decoupling and short return paths.
- All future designs should prioritize tight decoupling placement and continuous ground planes, as these design practices dramatically improve signal integrity and reduce switching noise.

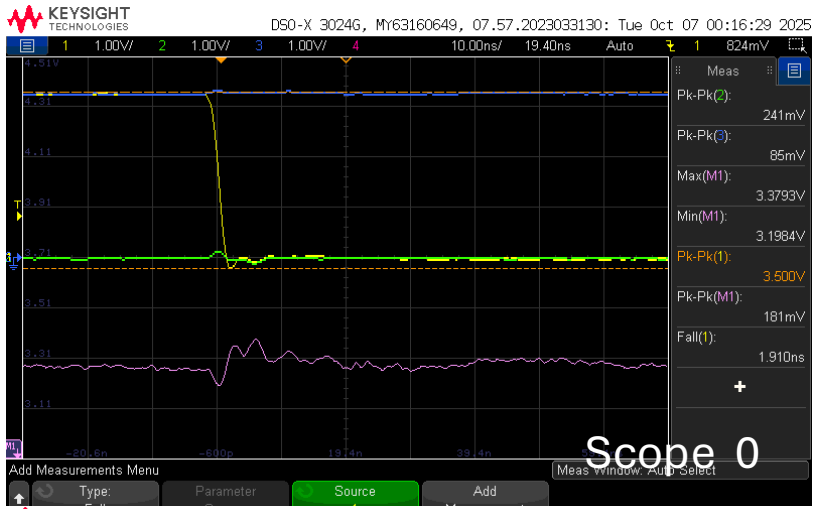
Full Results:

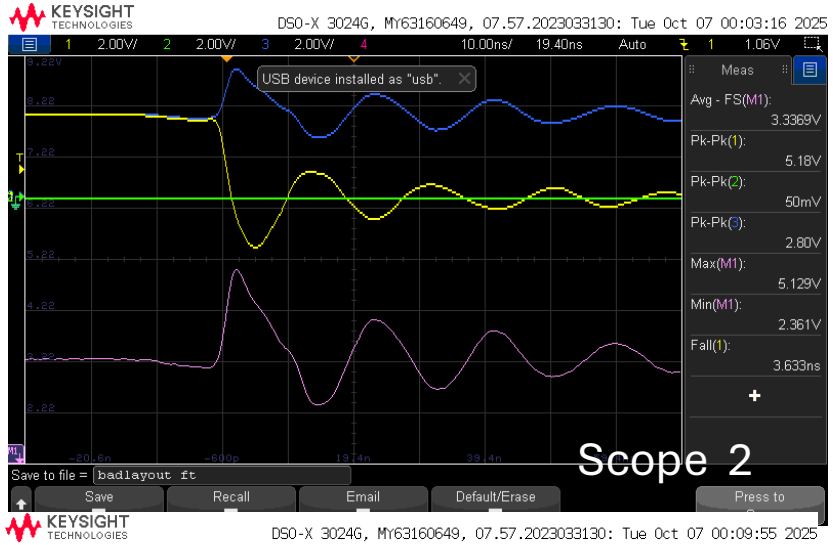
Layout	Rise Time (ns)	Voltage Rail Collapse (Pk–Pk mV)	Scope Ref.	Fall Time (ns)	Voltage Rail Collapse (Pk–Pk mV)	Scope Ref.
Good Layout	2.25	274	Scope 0	1.89	181	Scope 1
Bad Layout	4.86	1031	Scope 2	3.92	2763	Scope 3
Good but Cap Far	3.78	709	Scope 4	2.47	829	Scope 5

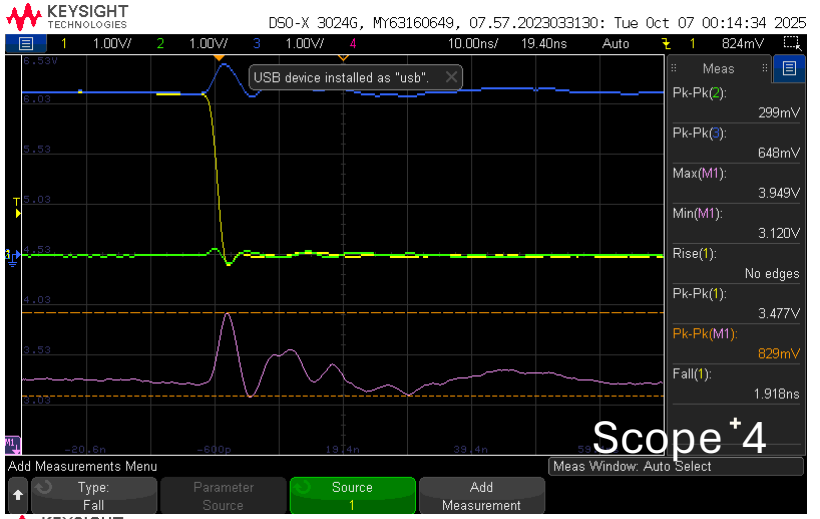


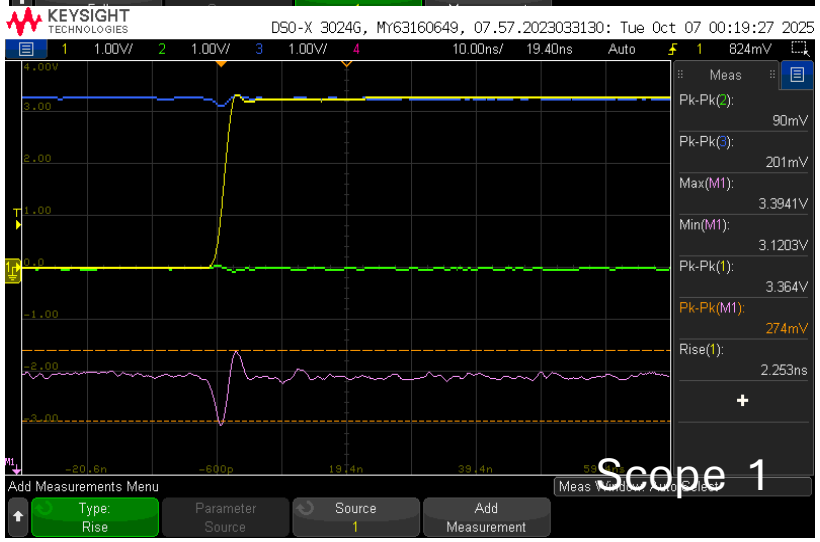
555 clock | Bad layout

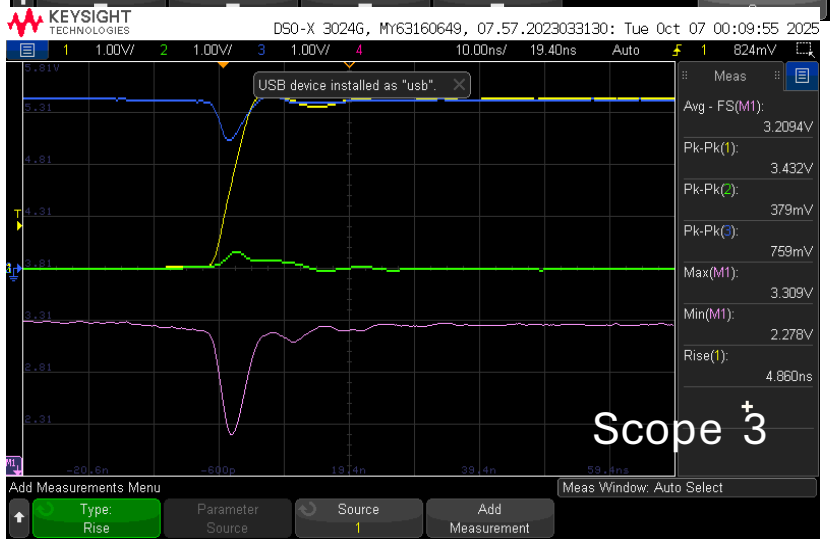
Good layout | Good but cap far











555 clock | Bad layout

Good layout | Good but cap far