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Board 2 report: Hex inverter

Objectives:

PCB LAYOUT DECISION
- SWICHING NOISE
- POWER DELIVERY NETWROK

The purpose of the board 2 is to demonstrate how the layout decisions lead to the best and worst switching noise on the PDN (Power Delivery Network. The board consists of two identical hex inverter circuits, one with good layout practices and the other with bad layout practices.

Using hex inverter, on-die power rail measurements that I measured the voltage directly on the chip's power line.

Plan of Record (POR):

The circuit should have,

- A power plug for "AC to 5V DC adaptor" to supply power for the board.

- 3.3 LDO for providing 3.3V for hex inverters and filter capacitor on its feedback with switch, to notice the difference in its presence and absence.
- A switch to select between 5V/3.3V supply for Hex inverters.
- A 555-timer circuit (Astable) designed to generate 5Vp-p square wave with 500Hz and 60% duty cycle which acts as clock for the hex inverters.
- Two hex inverter circuits are connected to 5V/3.3V switch.
- 3 LEDs connected to each hex inverter IC (to cause dI/dt) which are driven by the square wave of 555 timer.
- A pull up resistor of 10KΩ to prevent unintentional turning ON of LEDs due to noise when they are not driven by 555 outputs. (Because of high input impedance of inverter)
- Two inverters on each hex inverter are connected to supply and ground to measure on-die-switching noise: Quiet low and Quiet high.
- current limiting resistors for each hex inverter LEDs: 47Ω.
- Indicator LED for the power supply and LDO
- Test points for 5V rail, 3.3V, 555 timer output, and each inverter's 47 Ω resistor to measure current, Quiet low and Quiet high signals.

- Isolation header pins for 555 timer and each hex inverter.

Sketch of Circuit:

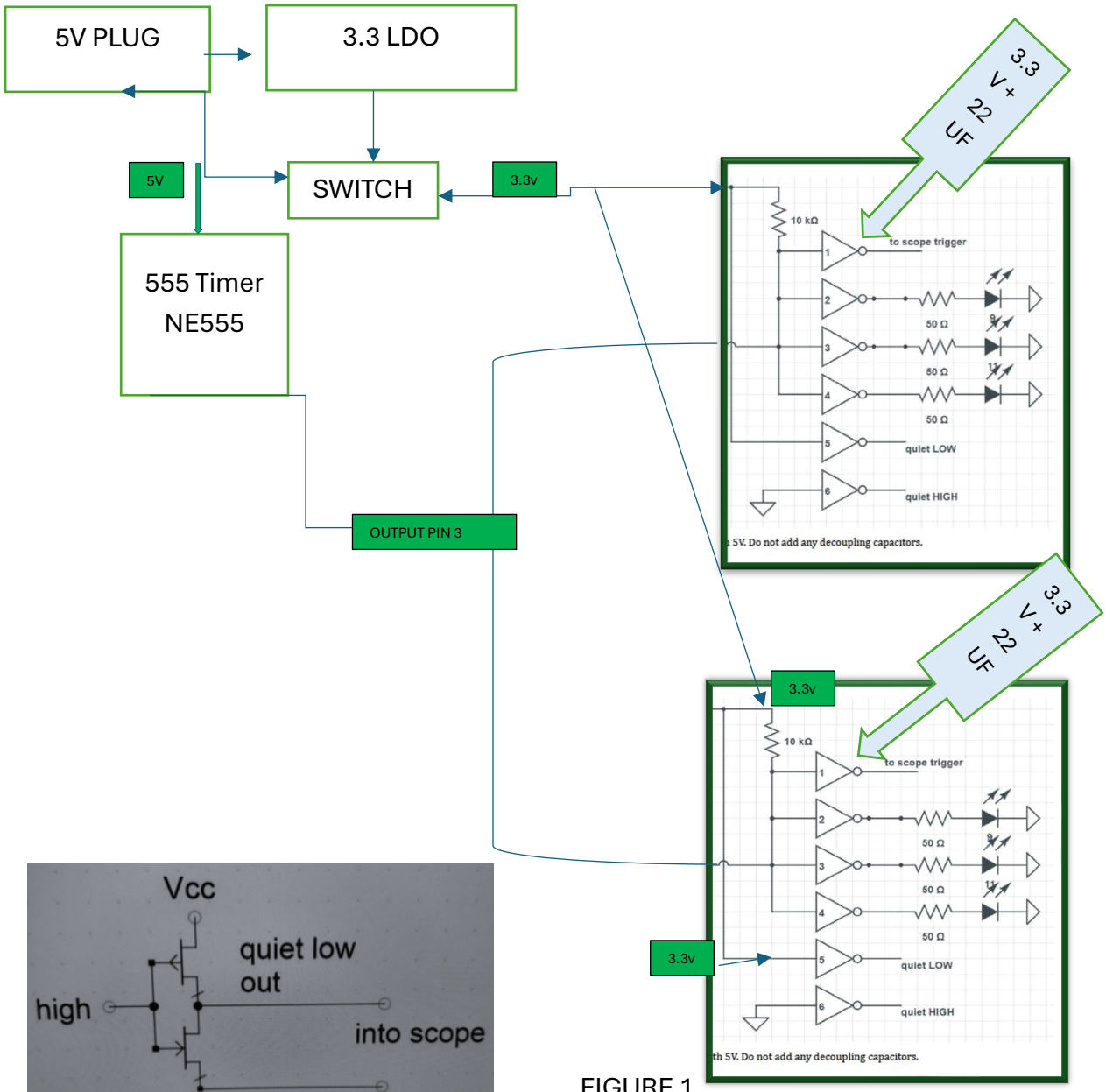

FIGURE 1

FIGURE 2: Transistor level circuit of an inverter

In FIGURE 1, it is evident that if the input of an inverter is tied to Vcc, then P-MOSFET is OFF and N-MOSFET is ON, causing VSS to be connected to the output always. Noise measured at the output is the direct measure of on-die VSS/GND noise (QUIET LOW). Similarly, if input of other inverter is connected to the ground, then its output is the direct measure of on-die VCC/Positive rail (Quiet high).

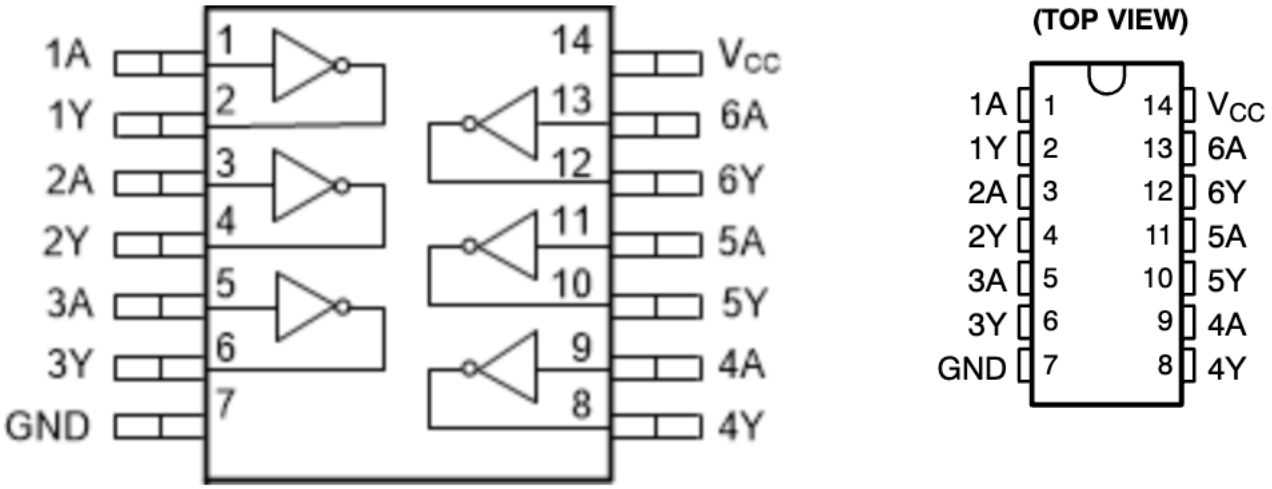

Figure 3: Hex Inverter from top view

Components selection calculations:

NE555 TIMER IC(BJT)

This model of timer can sink up 200mA, and it has output rise time =100ns

min input supply = 4.5v(from the datasheet)

The formula for the frequency of the output square wave and duty cycle of this timer are as follows:

$$f = \frac{1.44}{(Ra + 2Rb) * C}$$

To reduce Ra=Rb=1Kohm, and desirable frequency is 500KHZ. After solving, we obtain→ C=1UF

Duty cycle= $\frac{Ton}{Ton+Toff} = 0.693(Ra + Rb) * \frac{c}{[0.693(Ra+Rb)C]+0.693(Rb)c} = 66\%$

BOM/Components required:

1. 555 timer IC – NE555DR
2. LDO – AMS1117
3. Hex inverter – SN74AHC14DR
4. Resistor – 47Ω -6, 10k Ω-2 (pull-up), 1kΩ- 4 (for timing – 2, current limiting for indicator LED – 2)
5. LED – 8
6. Power Plug
7. Header pins for isolation.
8. Capacitor – 1µF (for 555 timer), 22µF – 5 (for decoupling – 4, for LDO feedback - 1)
9. Shorting flags for isolation switches.

Schematic:

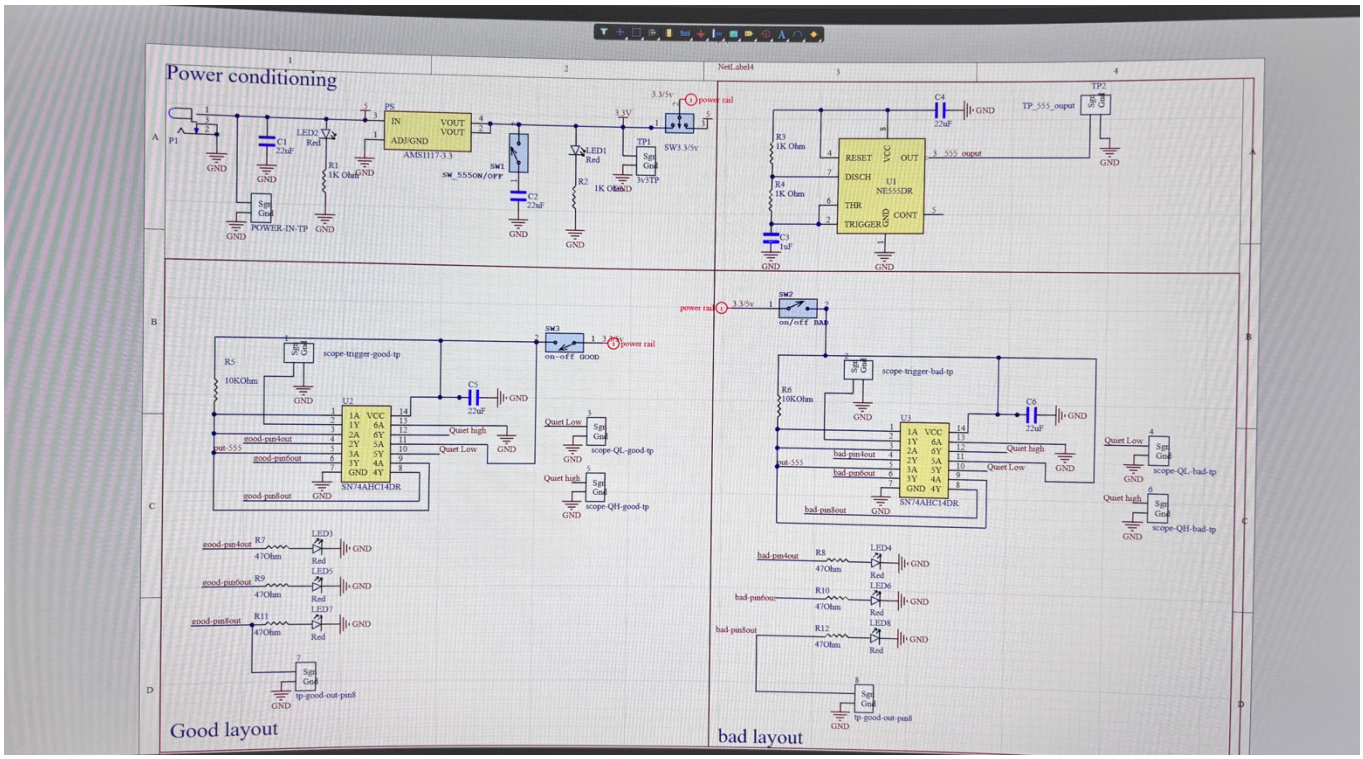

Figure 4: Hex inverter SCHEMATIC in Altium Designer

Layout:

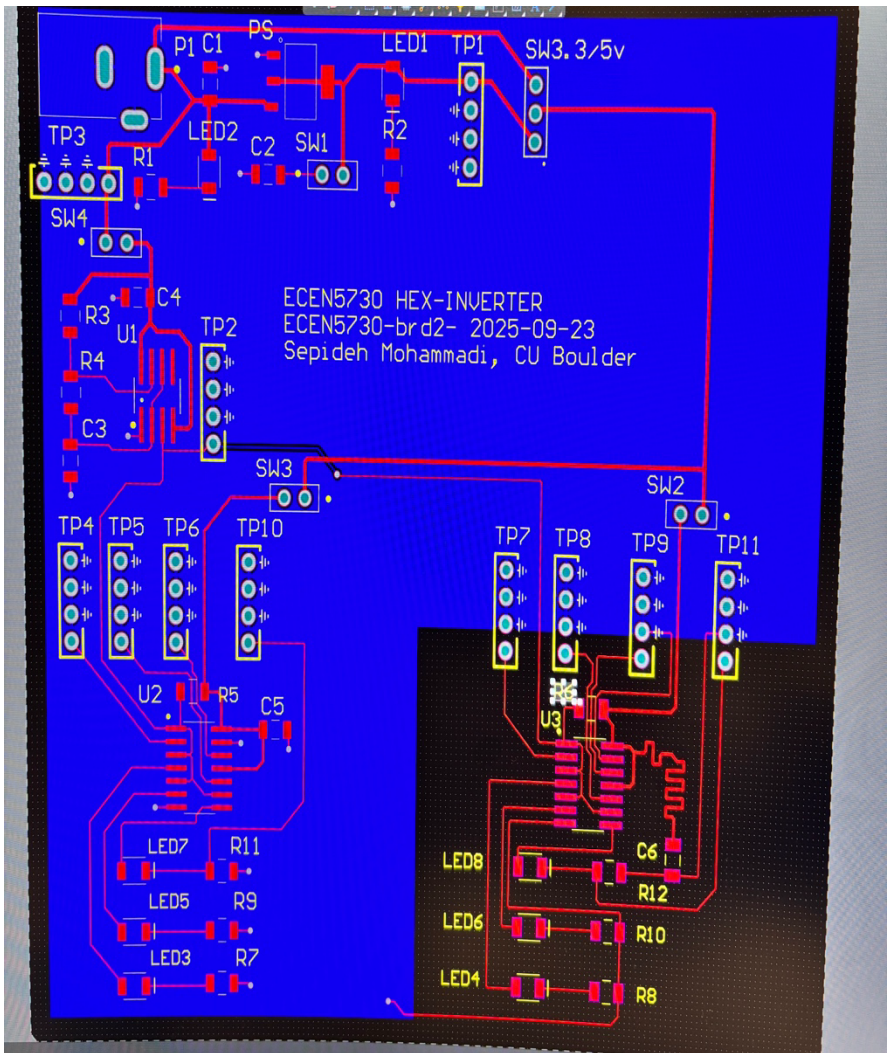

Figure 5: Hex inverter layout done in Altium Designer

The black part (right section/bad layout) which indicated that it has no bottom return place. all the returns are interconnected, and decoupling capacitor is far from the IC. On the left side bottom (Good layout), it has continuous plane on its bottom layer and the decoupling capacitor in near the IC.

After assembling manually:

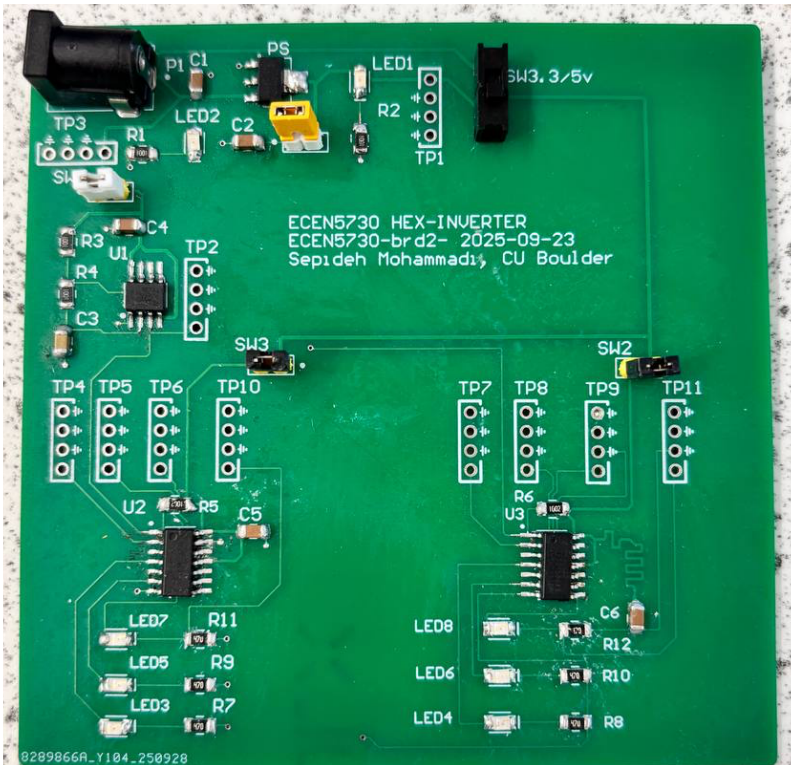

Figure 6: Top side assembled board.

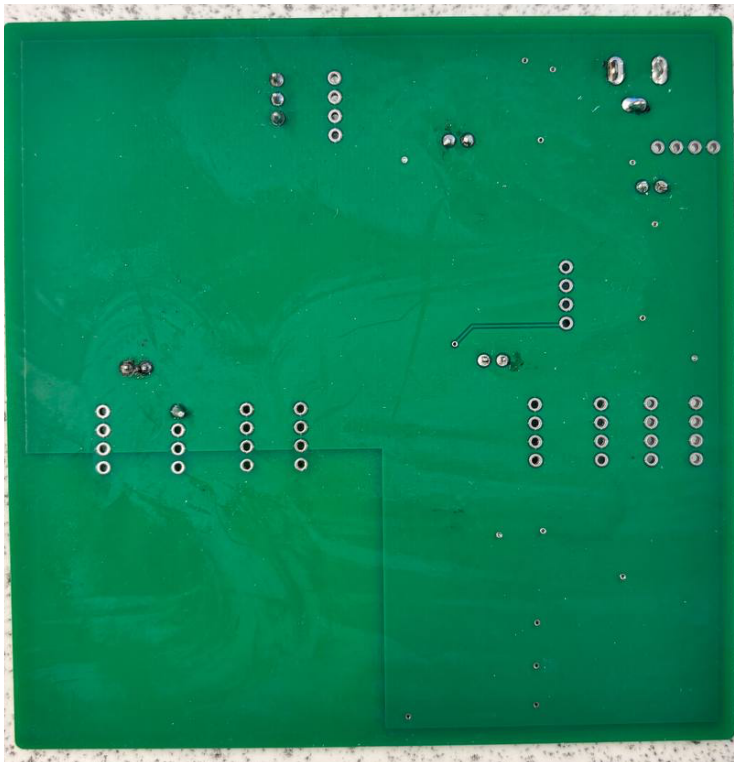

Figure 7: Bottom Side assembled board

What it means to work

1. When the power is on, indicator LEDs (5V and 3.3V) should turn ON.
2. Board is powered with a 5 V AC to DC adapter which can be measured at TP3 and 3.3V of LDO at TP1.
3. With SW4 ON near the TP3(white switch), the 555 timer outputs a square wave signal with a frequency and duty cycle of about 500 Hz and 66% and rise time is around 100 ns. This can be measured at the test point TP2.
4. With SW2, SW3 ON, 555 timer output should drive 3 LEDS of each inverter (Good and bad layout) and scope trigger can be measured (TP4, TP7)
5. 3 LEDs of each inverter should work on both 3.3V and 5V power supply switched by shorting flag at SW2.
6. Quiet low and Quiet high signals can be measured for each inverter (TP5, TP6, TP8, TP9)
7. TP5 and TP6 are for Good Layout, TP8 and TP9 are for bad layout
8. The current through the LED with 47Ω can be measured at test points TP10(Good Layout) and TP11(Bad Layout).

What worked/ Bring-up:

There were **no hard/soft errors**. The indicator LED of 5V, 3.3v supply, output LEDs turned ON, and all the test points can be measured.

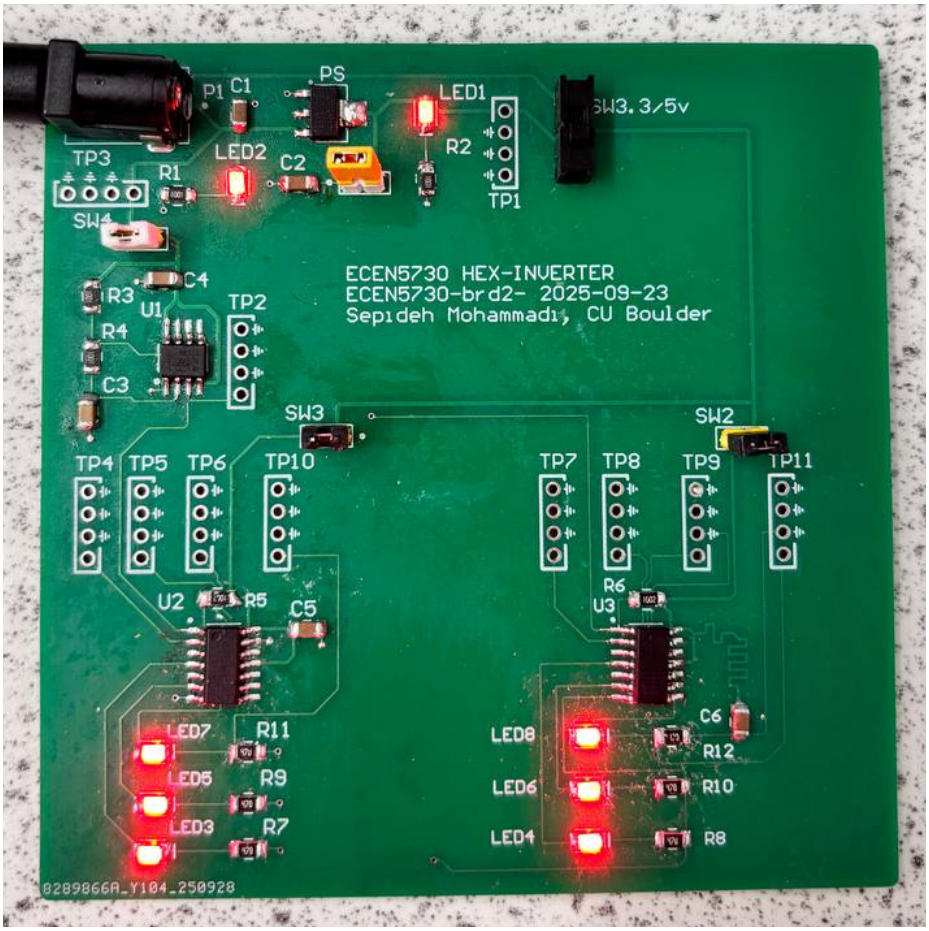

Figure 8: Fully Functioning Board

Scope Shots and Analysis:

1. Power Rail Measurement at TP2 and TP1 (5 V and 3.3 V Rails)

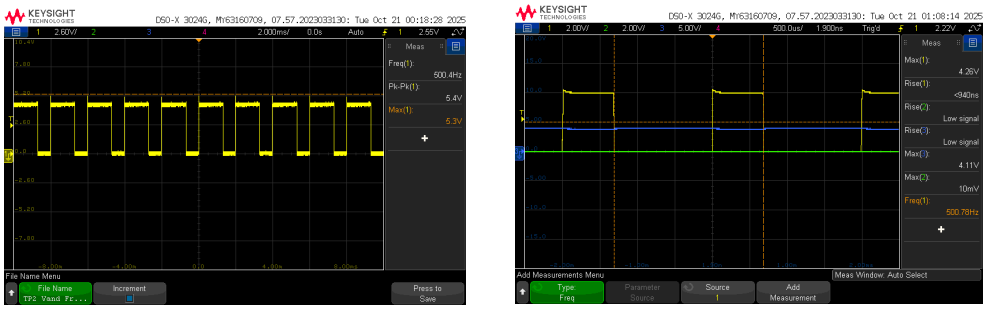

Figure 9 for both rails: Power rail in 5Vand 3.3 rail in the output of NE555 timer

Two supply rails were monitored to compare the output behavior of the NE555 timer and the corresponding rail stability. The 5 V rail was measured at TP2, and the 3.3 V rail was measured at TP1. The NE555 timer generated a square-wave clock of approximately 500 Hz, observed on both rails using identical time-base and voltage-scale settings for consistency.

The 555-timer output (yellow) is connected to one of the NOT gates of the hex inverter, and the inverter output serves as the trigger. When powered at 3.3 V, the inverter output (green) shows a 3.3 Vp-p square waveform that is inverted relative to the 555 outputs. Both waveforms maintain similar frequency (~500 Hz) and duty cycle, confirming proper triggering and rail regulation performance at both voltage levels.

2. 555 clock and triggers of Hex inverters

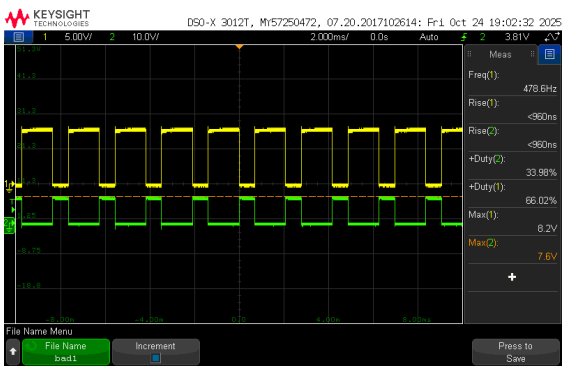

Figure 10: Bad Layout trigger to 5 v rail of timer

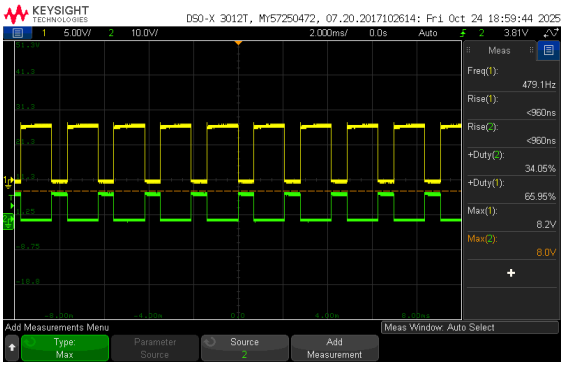

Figure 11: Good Layout trigger to 5 v rail of timer

2.1 In the bad layout (Figure 10), the timer output operates at 482.1 Hz with a rise time < 960 ns, fall time < 960 ns, and a duty cycle of 34.31 %, while the 5 V rail shows larger ripple up to 8.7 V p-p due to poor decoupling and ground return.

In the good layout (Figure 11), the signal frequency is 479.1 Hz with a rise time < 960 ns, fall time < 960 ns, and a duty cycle of 34.05 %, and the 5 V rail ripple reduces to about 8.0 V p-p, confirming improved stability and lower noise from proper layout design.

3. LDO oscillations during rising and falling edges: GOOD LAYOUT

Rising and Falling Edge – Quiet Low and Quiet High

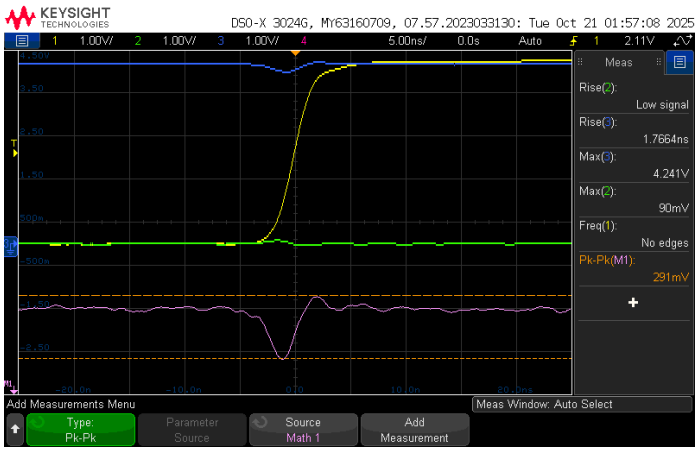

Figure 12: falling edge for Good layout

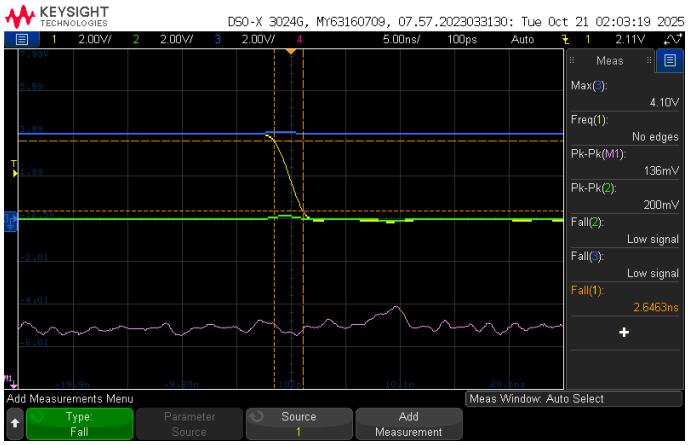

Figure 13: falling edge for Good layout

4. Rising edge (Figure 12): Channel 1 (yellow) is the inverter output triggered by the 555 clocks. The rail compression is 291 mV p-p with a rise time of 1.76 ns, showing stable switching and minimal noise due to proper decoupling.
   Falling edge (Figure 13): Rail compression is 136 mV p-p with a fall time of 2.64 ns, indicating low ground bounce and clean transitions in the good layout.

Measurements	Good Layout Rise time	Good Layout – Falling
Rise / Fall time (ns)	1.76	2.64
Quiet low: Vp-p (mV)	690	200
Quiet high: Vp-p (mV)	90	69
Rail compression: Vp-p (mV)	291	136

5. LDO oscillations during rising and falling edges: Bad LAYOUT
   Rising and Falling Edge – Quiet Low and Quiet High

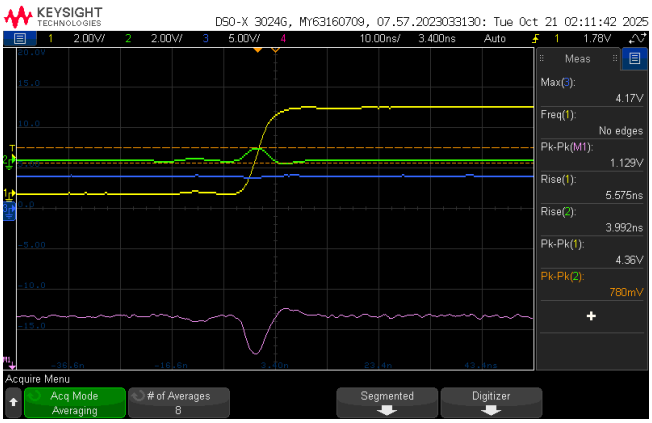

Figure 14: rising edge for bad layout

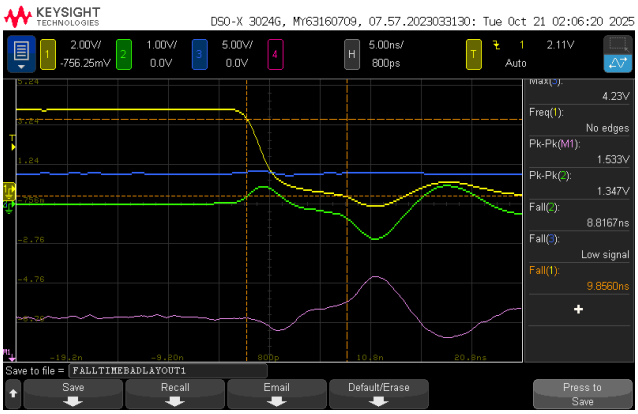

Figure 15: falling edge for bad layout

6. Bad Layout (Figures 14–15): The rise and fall times are 5.58 ns and 9.86 ns, respectively, with rail compression up to 1.5 V p-p and quiet-node noise exceeding 1 V p-p. The slower transitions and higher noise indicate poor signal integrity caused by long traces, inadequate return paths, and insufficient local decoupling, leading to noticeable ground bounce and supply disturbance during switching.

Measurement	**Rising Edge**	**Falling Edge**
Rise / Fall time (ns)	**5.58 ns**	**9.86 ns**
Quiet low Vp-p (mV)	**780 mV**	**1 347 mV**

Comparison: GOOD layout vs. Bad layout

Measurement	Good Layout	Bad Layout
Rise time (ns)	1.76 ns	5.58 ns
Fall time (ns)	2.64 ns	9.86 ns
Quiet low Vp-p (mV)	1347 mV	200 mV
Quiet High Vp-p (mV)	690	1900
Rail compression: Vp-p(v)	0.917	1.85

7. The good layout achieves much faster edge transitions (3× faster) and over 5× lower noise, confirming that short traces, local decoupling capacitors, and continuous ground return significantly improve power integrity and reduce ground-bounce effects in the inverter network.

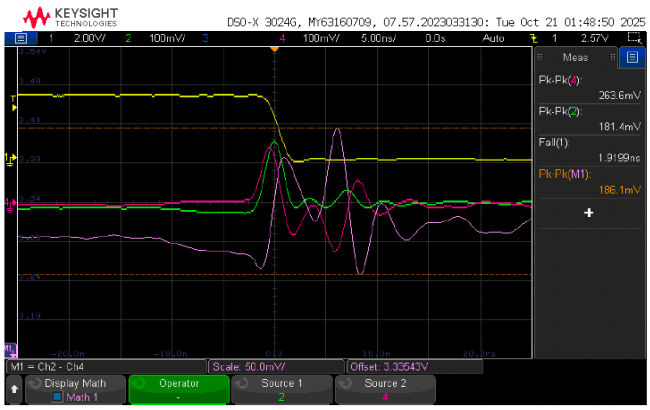

Figure 16: 3.3V Good layout falling edge rail collapse

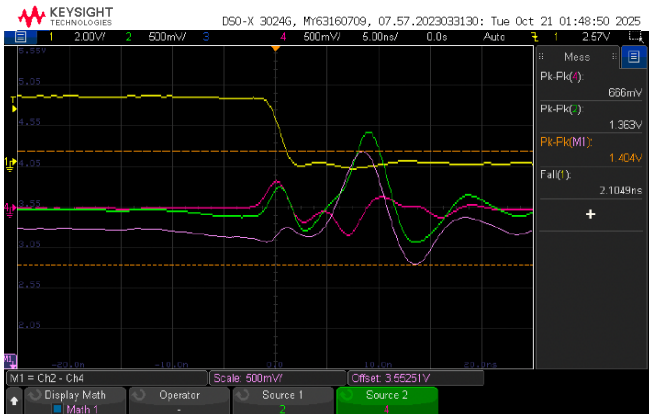

Figure 17:3.3V Bad layout falling edge rail collapse

Measurements	Good Layout (Figure 16)	Bad Layout (Figure 17)
Fall time (ns)	1.9	2.1
Quiet low Vp-p (mV)	263	666
Quiet high Vp-p (mV)	181	1360
Rail compression Vp-p (V)	0.19	1.4

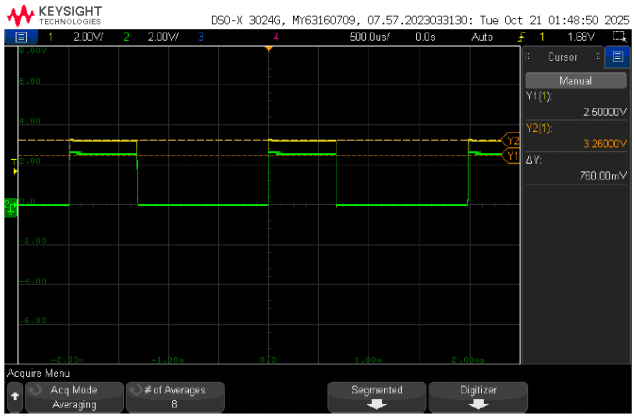

Figure 18: voltage across LED

8. Thevenin Resistance of the output of Hex inverter:

Rth = ((Vth-Vload)/Iload)
From Vth is the no-load voltage at inverter output = 3.3V Vload is the voltage at inverter output when the LED is driven in figure 18 = 2.56V
load = Voltage across 47 ohms/47 ohms = 0.565/47 = 12mA
Rth = (3.3-2.56) --→ Rth = 66Ω.

9. Best Design Practices Followed

1. The number of unique components was minimized during selection to simplify the design.
2. Decoupling capacitors were placed close to the ICs (except in the bad layout) to minimize loop inductance and stabilize the power rail.
3. Test points were clearly labeled to prevent connection errors.
4. Indicator LEDs and isolation switches were added to make debugging and testing easier.
5. A continuous ground return plane was used (except in the bad layout) to reduce crosstalk and noise.
6. Power traces were set to **20 mil** width for higher current capacity, while signal traces used **6 mil** width to maintain compact routing and low fabrication cost.

7. **1206** package components were chosen for easier manual soldering and assembly.

10. Conclusion

This board successfully demonstrates key PCB design practices such as placing decoupling capacitors near ICs and maintaining a continuous ground plane under signal traces. It also enabled direct observation of on-die power rail noise and its dependence on layout quality.