LAB 5 : SBB PDN and Slammer circuit

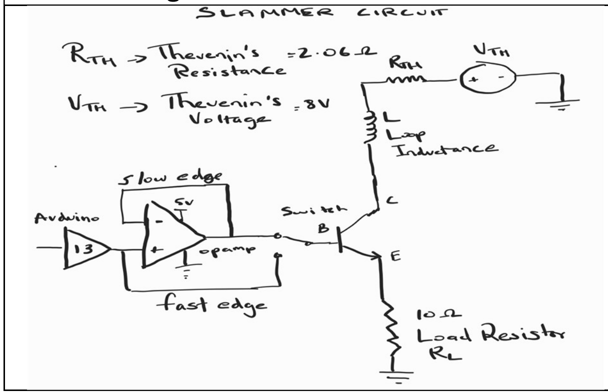
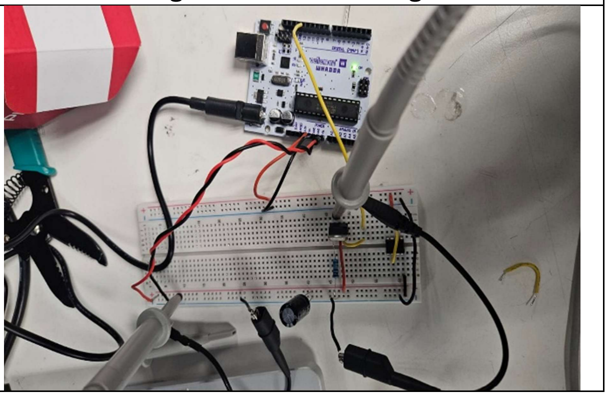
1. OBJECTIVES

- Build a breadboard prototype of a slammer circuit to draw sudden current and see how it affects the power rail.
- Observe, study, and find solutions for the effects of switching noise on the power rail.
- Learn the best ways to choose decoupling capacitors and how they help reduce switching noise.

2. COMPONENTS USED

1. Breadboard
2. TIP41C transistor
3. MCP601 op-amp
4. Arduino
5. 10 ohm resistor
6. Capacitors – 1000uF & 1uF

3. THEVENIN'S CIRCUIT AND CIRCUIT IMAGE

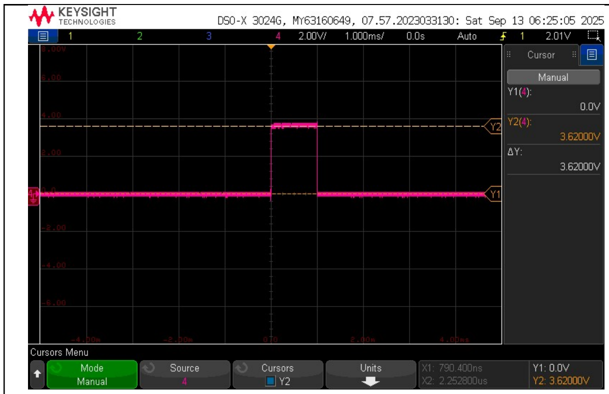
Figure 1 - Thevenin's circuit	Figure 2 - Circuit Image
	

4. DESCRIPTION OF THE CIRCUIT

We are building a Slammer circuit that suddenly pulls current from the power rail of 9V, similar to how an I/O port inside a chip works. An NPN transistor will be switched on by a $5V_{p-p}$ signal at a 5% duty cycle to drive a 10 Ω load resistor. To study the effect on the power rail, we will compare two types of control signals:

- A fast-rising signal with 4ns rise time directly from the Arduino.
- A slow-rising signal with 1.4us created by passing the Arduino output through an op-amp.

5. ESTIMATION OF LOAD CURRENT , THEVENIN’S VOLTAGE AND RESISTANCE


DSO-X 3024G, MY63160649, 07.57.2023033130: Sat Sep 13 06:25:05 2025

1 2 3 4 2.00V/ 1.000ms/ 0.0s Auto 1 2.01V

Y1(4): 0.0V

Y2(4): 3.62000V

ΔY: 3.62000V

X1: 790.400ns

X2: 2.252800us

Y1: 0.0V

Y2: 3.62000V

Figure 3 – Across 10ohms resistor

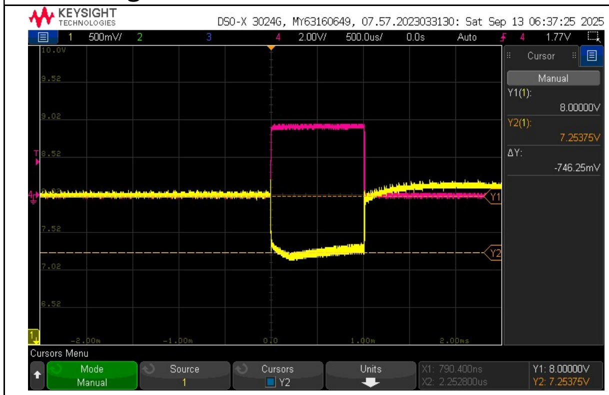
__Load Current__

Figure 3 measures the voltage drop across the 10 ohms load resistor (RL).

$$VLdrop = 3.62V$$

$$IL = \frac{VLdrop}{RL} = \frac{3.62}{10} = 0.362A$$

This current I_L is equal in the closed circuit so I_{th} (current through R_{th}) = I_L


DSO-X 3024G, MY63160649, 07.57.2023033130: Sat Sep 13 06:37:25 2025

1 500mV/ 2 3 4 2.00V/ 500.0us/ 0.0s Auto 4 1.77V

Y1(1): 8.00000V

Y2(1): 7.25375V

ΔY: -746.25mV

X1: 790.400ns

X2: 2.252800us

Y1: 8.00000V

Y2: 7.25375V

Figure 4 – Voltage drop due to R_{th}

__Thevenin’s voltage and resistance__

Figure 4 measures the Total voltage drop in the 9V power rail due to R_{th} without any decoupling capacitors.

The Thevenin’s voltage(V_{th}) is measured during the off time when no current is drawn.

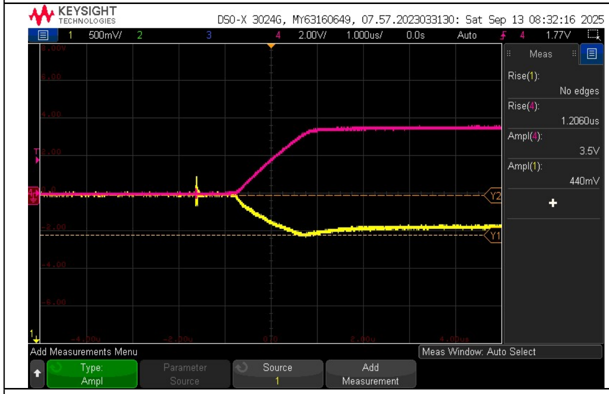
V_{th} = Voltage during off-time = 8V
V_L = Voltage during on-time = 7.253V

So, $Rth = \frac{Vth-V}{IL} = \frac{0.746}{0.362} = 2.06\ ohms$

6. LOOP INDUCTANCE AND SELECTION OF DECOUPLING CAPACITOR VALUE

Figure 5 & 6 measures the Voltage drop during slow edge and fast edge respectively

Figure 5 - Slow edge voltage drop with no capacitor


DSO-X 3024G, MY63160649, 07.57.2023033130: Sat Sep 13 08:32:16 2025

1 500mV/ 2 3 4 2.00V/ 1.000us/ 0.0s Auto 4 1.77V

Rise(1): No edges

Rise(4): 1.2060us

Ampl(4): 3.5V

Ampl(1): 440mV

Meas Window: Auto Select

__Loop Inductance__

$$L = \frac{V * dt}{di} = \frac{0.44 * 1.5 * 10^{-6}}{0.362} = 1.82uH$$

__Capacitance value for drop < 100mV__

$$C = \frac{I * dt}{dv} = \frac{0.362 * 1.5 * 10^{-6}}{0.1} = 5.43\text{uF}$$

Figure 6 - Fast edge voltage drop with no capacitor


DSO-X 3024G, MY63160649, 07.57.2023033130: Sat Sep 13 08:29:32 2025

1 500mV/ 2 3 4 2.00V/ 50.00ns/ 0.0s Auto 4 1.77V

Rise(1): No edges

Rise(4): 109.6ns

Ampl(4): 3.9V

Ampl(1): 1.80V

Meas Window: Auto Select

__Loop Inductance__

$$L = \frac{V * dt}{di} = \frac{1.8 * 100 * 10^{-9}}{0.362} = 0.497uH$$

__Capacitance value for drop < 400mV__

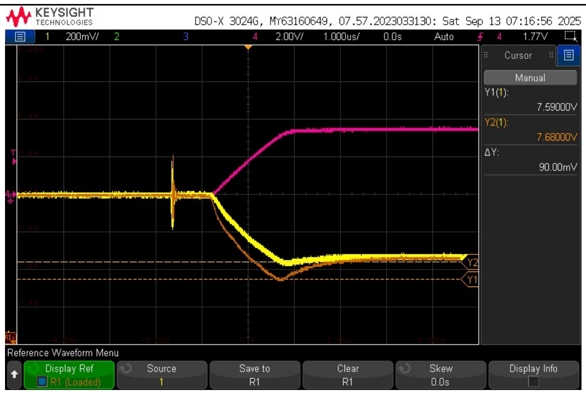
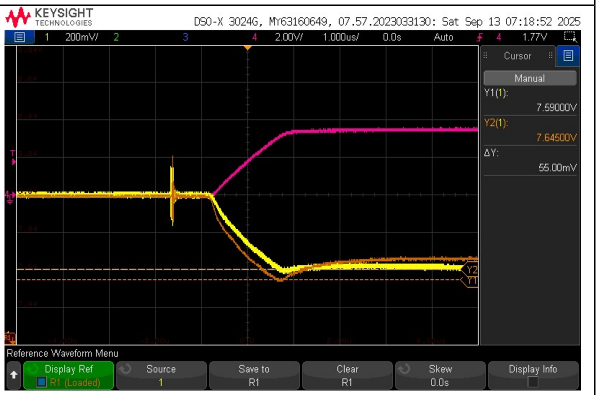
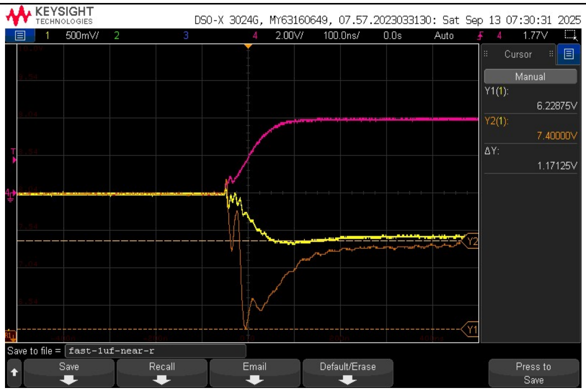
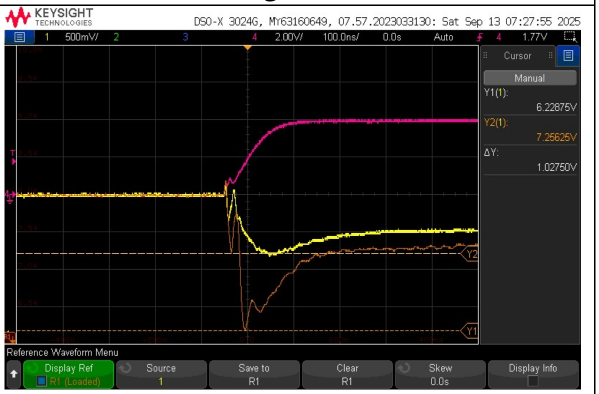
$$C = \frac{I * dt}{dv} = \frac{0.362 * 100 * 10^{-9}}{0.4} = 90.5nF$$

7. VOLTAGE DROP WITH 1UF AND 1000UF CAPACITORS

In Figures 7–14, the pink channel illustrates the output waveform across the load resistor. The brown channel, stored in memory as a reference, shows the voltage drop during the di/dt period in the absence of a decoupling capacitor. In comparison, the yellow channel displays the voltage drop during the di/dt period when a 1 μF & 1000 μF decoupling capacitor is placed on the power rail. This allows a direct observation of the improvement provided by the capacitor under different edge conditions.

1. 1UF CAPACITOR WITH NEAR AND FAR EFFECT.

A 1 μF capacitor is connected to the 9 V power rail. Two cases are studied: one with the capacitor placed far from the transistor and the other with it placed close to the transistor. The effects are observed for both slow and fast signal edges.

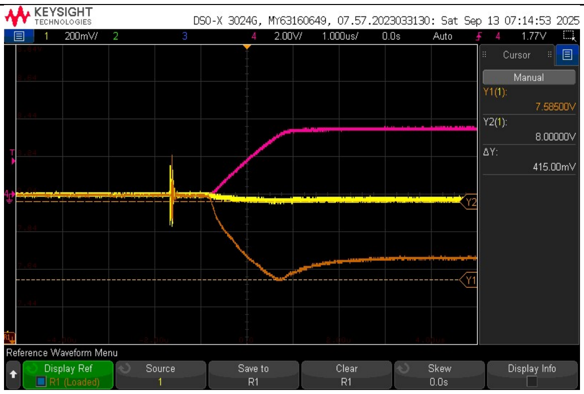
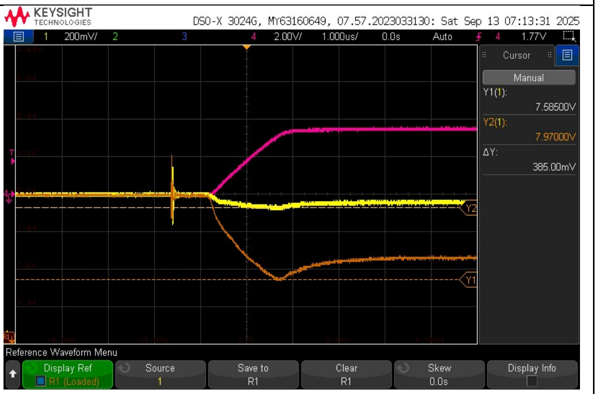
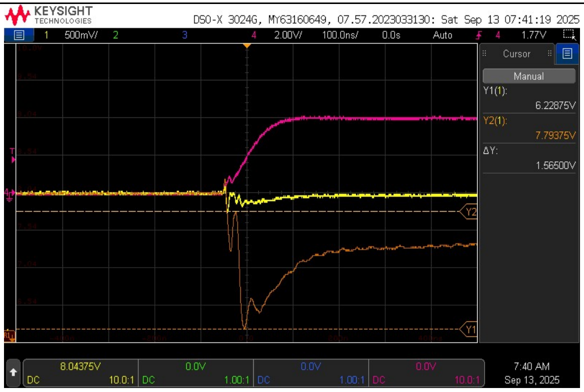
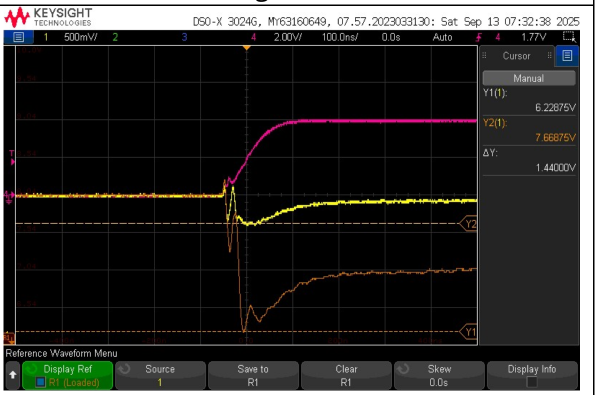
	Near Transistor	***Far from transistor***
Slow edge	 DSO-X 3024G, MY63160649, 07.57.2023033130: Sat Sep 13 07:16:56 2025 Y1(1): 7.59000V Y2(1): 7.68000V ΔY: 90.00mV *Figure 7*	 DSO-X 3024G, MY63160649, 07.57.2023033130: Sat Sep 13 07:18:52 2025 Y1(1): 7.59000V Y2(1): 7.64500V ΔY: 55.00mV *Figure 8*
Fast edge	 DSO-X 3024G, MY63160649, 07.57.2023033130: Sat Sep 13 07:30:31 2025 Y1(1): 6.22875V Y2(1): 7.40000V ΔY: 1.17125V Save to file = fast-1uf-near-r *Figure 9*	 DSO-X 3024G, MY63160649, 07.57.2023033130: Sat Sep 13 07:27:55 2025 Y1(1): 6.22875V Y2(1): 7.25625V ΔY: 1.02750V *Figure 10*

Below table shows the improvement in voltage drop with respect to the placement of the decoupling capacitor.

	Near Transistor	*Far from transistor*
Slow edge	*Y1 → 7.59V* *8.04V – 7.59V = 450mV drop without decoupling capacitor* *Y2 → 7.69V* *8.04V – 7.69V = 360mV drop with 1uF decoupling capacitor* *Total improvement = 90mV*	*Y1 → 7.59V* *8.04V – 7.59V = 450mV drop without decoupling capacitor* *Y2 → 7.645V* *8.04V – 7.645V = 395mV drop with 1uF decoupling capacitor* *Total improvement = 55mV*
Fast edge	*Y1 → 6.23V* *8.04V – 6.23V = 1.811V drop without decoupling capacitor* *Y2 → 7.4V* *8.04V – 7.4V = 640mV drop with 1uF decoupling capacitor* *Total improvement = 1.171V*	*Y1 → 6.23V* *8.04V – 6.23V = 1.811V drop without decoupling capacitor* *Y2 → 7.256V* *8.04V – 7.256V = 784mV drop with 1uF decoupling capacitor* *Total improvement = 1.027V*

2. 1000uF CAPACITOR WITH NEAR AND FAR EFFECT.

A 1000 µF capacitor is connected to the 9 V power rail. Two cases are studied: one with the capacitor placed far from the transistor and the other with it placed close to the transistor. The effects are observed for both slow and fast signal edges.

	Near Transistor	*Far from transistor*
Slow edge	 *Figure 11*	 *Figure 12*
Fast edge	 *Figure 13*	 *Figure 14*

Below table shows the improvement in voltage drop with respect to the placement of the decoupling capacitor.

	Near Transistor	*Far from transistor*
Slow edge	*Y1 → 7.59V* *8.04V – 7.585V = 455mV drop without decoupling capacitor* *Y2 → 8V* *8.04V – 8V = 40mV drop with 1000uF decoupling capacitor* *Total improvement = 415mV*	*Y1 → 7.59V* *8.04V – 7.585V = 455mV drop without decoupling capacitor* *Y2 → 7.97V* *8.04V – 7.97V = 70mV drop with 1000uF decoupling capacitor* *Total improvement = 385mV*
Fast edge	*Y1 → 6.23V* *8.04V – 6.23V = 1.811V drop without decoupling capacitor* *Y2 → 7.79V* *8.04V – 7.79V = 246mV drop with 1000uF decoupling capacitor* *Total improvement = 1.565V*	*Y1 → 6.23V* *8.04V – 6.23V = 1.811V drop without decoupling capacitor* *Y2 → 7.67V* *8.04V – 7.67V = 371mV drop with 1uF decoupling capacitor* *Total improvement = 1.440V*

7. OBSERVATIONS & CONCLUSIONS

OBSERVATIONS

1. **Switching Noise Impact**

- Without a decoupling capacitor, the 9 V rail showed a large voltage drop especially during fast signal edges. This happened because of the loop inductance between the source and the transistor.
- The drop was more severe for the fast-rising edge (1.811 V) compared to the slow-rising edge (450 mV), confirming that higher di/dt transitions has more impact on the PDN.

2. **Effect of Capacitor Value**

- The 1 µF capacitor provided partial improvement but was insufficient to fully stabilize the rail during fast edges.
- The 1000 µF capacitor showed a much stronger suppression of voltage drop, reducing it by more than 1.5 V during fast edges.

3. **Placement of Capacitor**

- Capacitors placed **close to the transistor** consistently gave better results than those placed far away, as expected from **reduced loop inductance**.
- The improvement margin was more pronounced for the fast-edge case.

CONCLUSIONS

- Decoupling capacitors are essential to suppress voltage droop caused by sudden current transients in power rails.
- Both value and placement of the capacitor are critical. A higher capacitance near the switching device significantly reduces supply noise.
- Our goal should be to use the **highest possible capacitance (to support transients)** in the **smallest package size (to minimize lead inductance)**, while keeping the **cost reasonable**.
- The path from the power source to the load should be kept as short as possible to reduce loop inductance, which adds to the voltage drop.